Оптический журнал

Оптическое приборостроение

Новая схема полностью оптического переключателя на основе двухбитовых комбинаций, кодируемых частотой, и результаты ее моделирования

© 2017 г. P. P. Sarkar*, M. Tech.; B. Ghosh*; S. N. Patra**, Ph. D & Prof.; S. Mukhopadhyay***, Ph. D

*Department of Electronics and Communication Engineering, University Institute of Technology, University of Burdwan, West Bengal, India.
**Department of Instrumentation Science, Jadavpur University, Kolkata-, West Bengal, India
***Department of Physics, University of Burdwan, West Bengal, India

Сверхскоростные полностью оптические элементы памяти и оптические логические схемы являются основными блоками при построении оптических вычислительных и коммуникационных систем. Реализация сверхскоростных ячеек памяти, работающих в оптическом диапазоне, является весьма многообещающей. В последнее время многими авторами предложены различные теоретические подходы для создания оптических триггеров и ячеек памяти, основанных на комбинационных и последовательных логических схемах. Предложена новая схема полностью оптического переключателя на основе двухбитовых комбинаций, кодируемых частотой, использующая отражательный полупроводниковый оптический усилитель и мультиплексор ввода-вывода, и выполнено корректное моделирование этой схемы. Использование техники двойного битового представления в сочетании с кодированием оптической частотой делает систему высокоскоростной, ведет к уменьшению цифровых ошибок и увеличению отношения сигнал/шум.

Ключевые слова: *оптические вычисления, нелинейная оптика, отражательный полупроводниковый оптический усилитель, мультиплексор ввода-вывода, двойные битовые оптические логические схемы, Симулинк.*

A new scheme of all optical frequency encoded DIBIT based latch with its simulated result

© 2017 г. P. P. Sarkar*, M. Tech.; B. Ghosh*; S. N. Patra**, Ph. D & Prof.; S. Mukhopadhyay***, Ph. D

*Department of Electronics and Communication Engineering, University Institute of Technology, University of Burdwan, West Bengal-713104, India.
**Department of Instrumentation Science, Jadavpur University, Kolkata-700032, West Bengal, India
***Department of Physics, University of Burdwan, West Bengal-713104, India

E-mail: pratim34@gmail.com, bitanghosh87@gmail.com, sankar.journal@gmail.com, sourangshu2004@gmail.com

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Super fast all optical memory and optical logic gates are the basic building blocks for optical computation and communication systems. Realization of a very fast memory-cell in the optical domain is very challenging. Recently different theoretical proposals based on combinational and sequential logic circuits for developing all optical flip flops as well as memory cells have been reported by the different authors. Here, the authors have proposed a new scheme of all optical frequency encoded dibit based latch circuit using reflected semiconductor optical amplifier and add/drop multiplexer with its proper simulation. The use of dibit representation technique along with optical frequency encoding technique makes the system very fast, reduce bit error problem and increase signal to noise ratio.

Keywords: *optical computation, non-linear optics, reflected semiconductor optical amplifier, add/drop multiplexer, dibit based optical logic gates, Simulink .*

OCIS codes: *190.0190, 190.4360*

1. INTRODUCTION

All optical data processing technique is the most alternative and successful replacement to overcome the speed related problems as light has the inherent character of parallelism [1]. Different types of all optical logic gates and memory circuits are the fundamental building blocks for optical data processors and communication systems [2–4]. Again, dibit representation technique provides the benefits of low bit error problem by increasing high signal to noise ratio. Here, the authors have proposed a new scheme of all optical frequency encoded latch by reflected semiconductor optical amplifier (RSOA) and add/drop multiplexer (ADM) blocks with dibit representation technique [5], where digital value '0' is represented as [0][1] logic states and digital value '1' is represented as [1][0] respectively. In other way, the presence of the two frequencies side by side [ν_1][ν_2] represents digital logic state '0' and [ν_2][ν_1] does the same as digital logic state '1'. To implement the all optical dibit based latch circuit, RSOA and ADM are two important optical switches, which are discussed bellow.

1.1. Reflected semiconductor optical amplifier

Reflected semiconductor optical amplifier is an optical switch [6], which is shown in Fig. 1. If a weak probe beam of light of ν_1 frequency and a strong pump beam of light of ν_2 frequency are inserted to the input terminals, then this block will provide the output beam in form of frequency of probe beam along with the power of the pump beam. Here, it will provide the output light beam of ν_1 frequency. But, if the frequencies of the pump and probe beam of light are interchanged, then opposite incident happens, i.e. now, it will provide the output light beam of ν_2 frequency. So, this could be established as a very promising optical device for conducting many all-optical logical operations.

1.2. Add/drop multiplexer

Optical ADM [7] is a frequency selective switch. Now, if it is tuned with a particular biasing current (I_1, I_2 etc.) then it reflects a particular frequency of light and passes all other frequencies of light. If it is biased by I_1 biasing current then it reflects ν_1 frequency of light beam and passes all other frequencies of light beams. But when it is biased by I_2 biasing current then it reflects ν_2 frequency of light beam and passes all other frequencies of light beams. Different incident happens if the biasing current changes. This block is shown in Fig. 2.

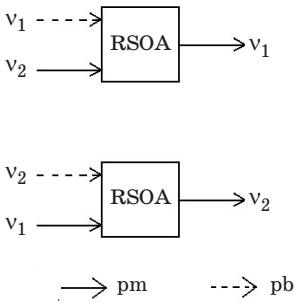

Fig. 1. Block diagram of RSOA. Probe beam — pb, pump beam — pm.

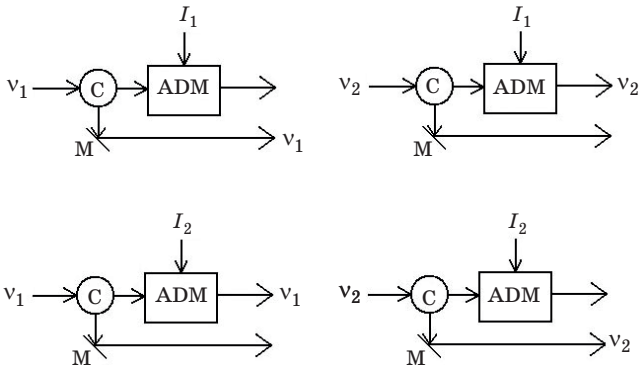

Fig. 2. Block diagram of ADM. C — calculator, M — mirror.

2. PRINCIPLE OPERATION OF FREQUENCY ENCODED ALL OPTICAL NOT BASED DIBIT LATCH

To develop a complete unit of frequency encoded all optical memory cell, the first step is to develop a latch or a memory unit as it can store a dibit. The proposed system described here is based on frequency encoding principle, shown in Fig. 3. Here we have used dibit representation technique [8]. So, dibit state [0][1] or [ν_1][ν_2] represents digital logic state '0' and dibit state [1][0] or [ν_2][ν_1] represents digital logic state '1'. Here, in our proposed system, 'I′' and 'I″' represents 1st bit and 2nd bit of dibit input and 'O′' and 'O″' are the dibit output terminals respectively. For better understanding about the state change of the latch circuit, we have considered the NOT logic gate based system. To implement the optical NOT based latch logic with dibit technique, beam splitters, mirrors, RSOA and ADM are used at different position of the system.

Here, optical wave beams in form of 'I′' = ν_1 and 'I″' = ν_2 frequencies are applied at input terminal, now, ν_1 frequency of light beam is moved as weak probe beam and ν_2 frequency of light beam is sent as strong pump beam to the $RSOA_1$. So, according to the principle of RSOA, we get ν_1 frequency of light beam at the output of $RSOA_1$. This frequency of light beam enters to ADM_1, which is biased by I_2 biasing current. So it passes ν_1 frequency of light beam to $RSOA_2$ as a pump beam. But there is a constant probe beam of ν_2 frequency of light beam at $RSOA_2$. For this reason output becomes in form of ν_2 frequency of light beam and goes to output terminal 'O′'.

Again a portion of this output frequency of light beam goes to $RSOA_3$ as a pump beam by the feedback path. Since there is a constant source of probe beam of ν_1 frequency of light, so ν_1 frequency of light beam comes out from $RSOA_3$ and this light beam of ν_1 frequency goes to another output terminal 'O″'. Now, to sustain the output continuously, there is a feedback process, where the output light beam of ν_1 frequency from 'O″' goes to the pump beam terminal of $RSOA_2$. After getting both the inputs, $RSOA_2$ provides ν_2 frequency of light beam at the output terminal which comes again in form of output to 'O′' and from this light a portion of light beam comes again to the $RSOA_3$, where there is a fixed input in form of probe beam. So, this $RSOA_3$ block again produces ν_1 frequency of light beam at the output. In this way, we get continuous output of ν_2 and ν_1 frequencies of light beam at the terminal 'O′' and 'O″' respectively with given $[\nu_1][\nu_2]$ input, and this output sustains, even if the input frequency of light beam is absent.

Now, if we apply optical light beam in form of 'I′' = ν_2 frequency and 'I″' = ν_1 frequency at input terminal. This input light beam is opposite of the first case. It is noticed that ν_2 frequency and ν_1 frequency of light beam are moved as weak probe beam and strong pump beam to the $RSOA_1$ respectively. According to the principle of RSOA, it provides ν_2 frequency of light beam at the output of $RSOA_1$ and it comes to the input terminal of the ADM_1. Here, ν_2 frequency of light beam is reflected by ADM_1 because it is biased by optical light beam of ν_2 frequency. So ν_2 frequency of light goes to $RSOA_4$ as a pump beam. Here, there is a constant probe beam in form of ν_1 frequency of light beam. Then output becomes ν_1 frequency of light beam and this light of ν_1 frequency goes to output terminal 'O′'. Now a part of this output light beam from the output of $RSOA_4$ goes to $RSOA_5$ as a pump beam by the feedback path, where there is a constant probe beam of ν_2 frequency of light. So, ν_2 frequency of light beam coming from $RSOA_5$ goes to output terminal 'O″'. Again, a portion of this output of light beam from 'O″' goes to the pump beam terminal of $RSOA_4$. So, the output is maintained incessantly by this feedback process. Here, we get continuous output of ν_1 and ν_2 at the terminal 'O′' and 'O″' respectively, that means as it is NOT based latch circuit, so, with given input of light beam in form of $[\nu_2][\nu_1]$, we get at the output of light beam in form of $[\nu_1][\nu_2]$. The output frequencies at both the terminals remain unchanged until or unless the input frequencies of light beams are altered. This is the overall configuration of the whole scheme [9].

Now, to describe the operation, it can be said that when dibit logic state [0][1] is applied at the input terminal, the upper portion of the proposed scheme (shown in Fig. 3) is activated but lower half does not. So one can ensure the ν_2 and ν_1 frequency of light beam come at the output terminal 'O′' and 'O″' respectively i.e. 'O′' = digital logic state '1' and 'O″' = digital logic state '0'. So, dibit logic state [1][0] is obtained at the output terminal of this latch circuit. Similarly, when dibit logic state [1][0] is applied at the input terminal, the upper half does not get active but the lower portion of the system is activated. Again, we get the output 'O′' = digital logic state '0' and 'O″' = digital logic state '1', i. e. dibit logic state [0][1] is obtained. The input and output of the optical dibit based latch or memory cell is also shown in the

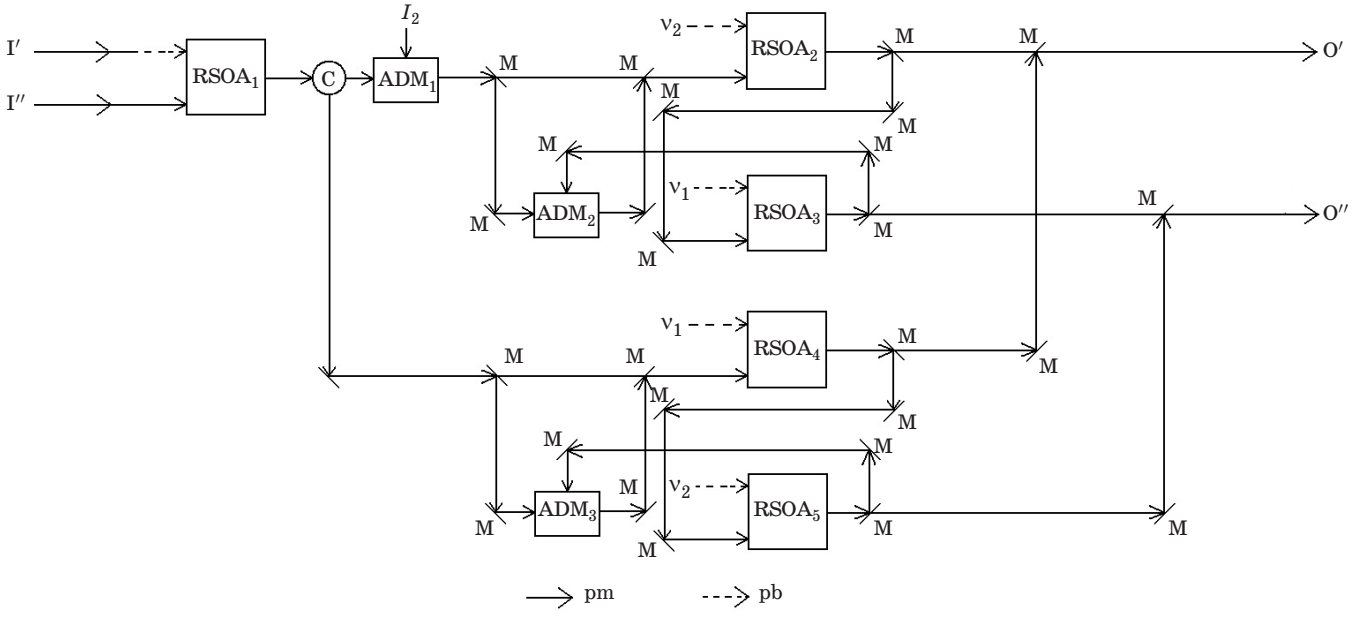

Fig. 3. Block diagram of frequency encoded NOT based dibit latch. C — calculator, M — mirror.

truth table (Table), which satisfies the fundamental logic principle of NOT based latch. Now, the most important and interesting point here is that if dibit logic state [0][1] or [1][0] are withdrawn from input terminal of this latch circuit, this scheme will continue to show the last attended values at the output terminal 'O'' and 'O''' simultaneously, as the final output due to the feedback mechanisms. So, it can be said that, the proposed scheme behaves as a frequency encoded all optical dibit based memory cell.

3. METHOD OF SIMULATION OF THE NOT BASED DIBIT LATCH

Now, following the block diagram of Fig. 3, we have simulated the dibit based optical latch circuit with MATLAB Simulink programming software in Fig. 4, where there are two output terminals, which provide the changeable output depending on the variation of inputs. Like, if we provide the dibit based input [ν_1] [ν_2] or [0][1] (here [3][8]) this simulated block provides the output in form of [ν_2][ν_1] or [1][0] (here [8][3]), as

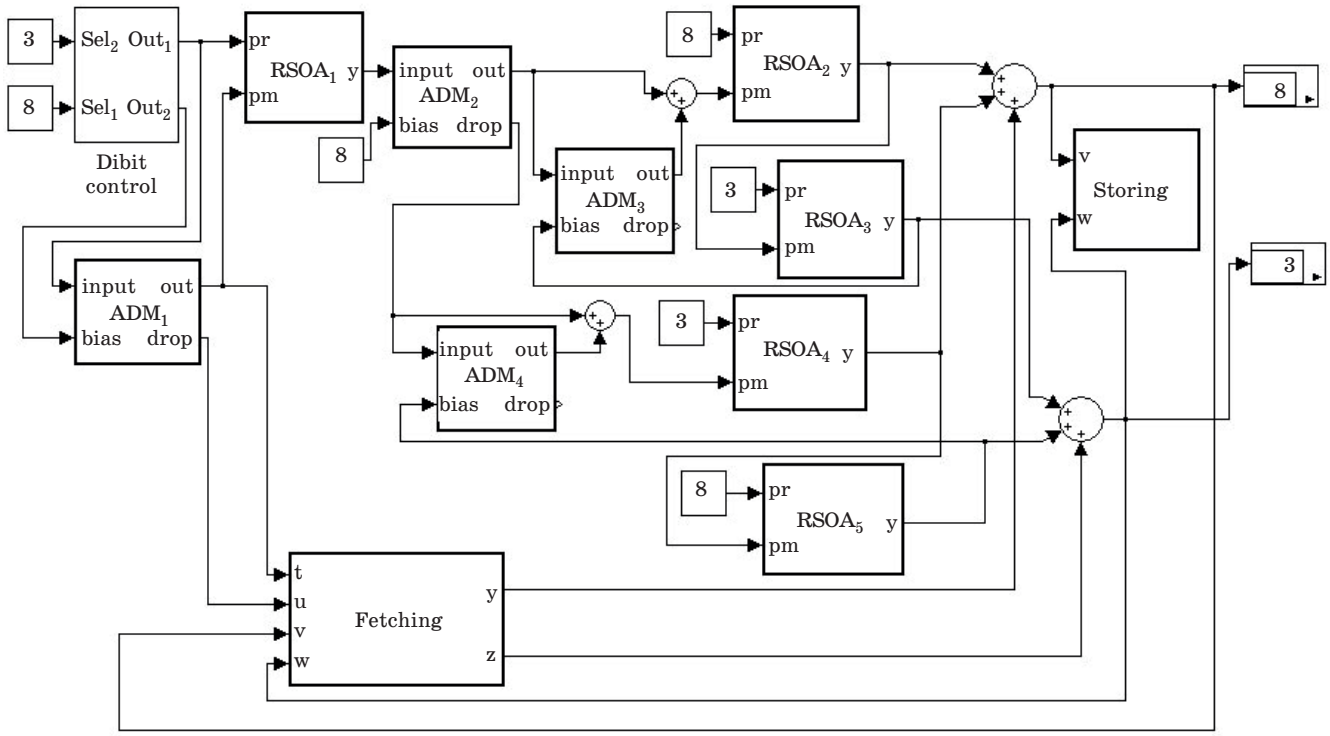

Fig. 4. Mathematical model of all optical frequency encoded NOT based dibit latch. Frequency 3 = ν_1 = DS = 0, frequency 8 = ν_2 = DS = 1, DS — digital state, pb — probe beam, pm — pump beam.

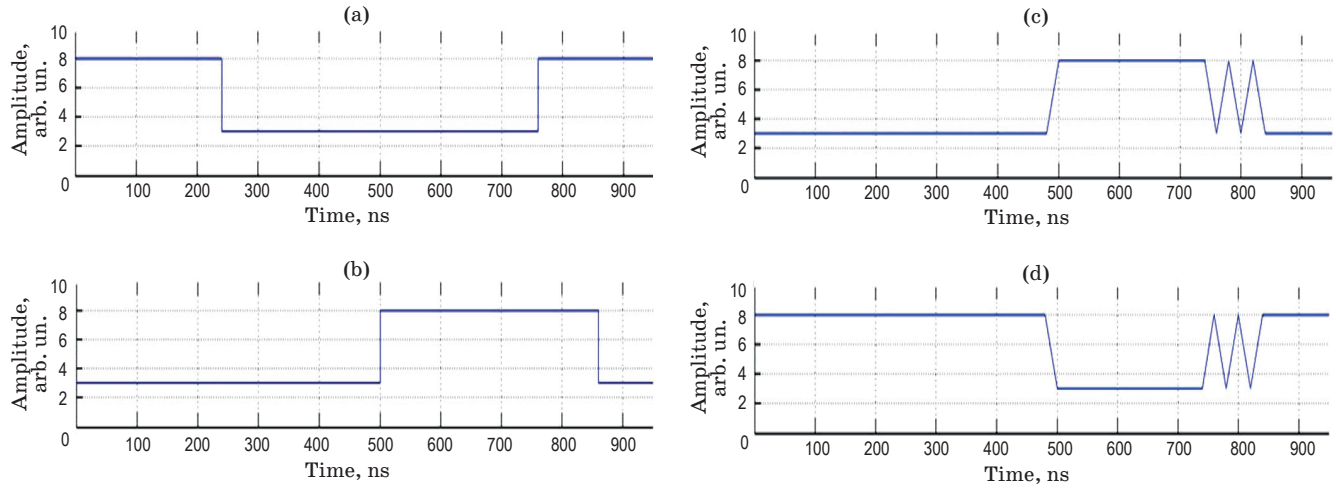

Fig. 5. Mathematical model of all optical frequency encoded NOT based dibit latch. (a, b) Dibit input (a — I′, b — I″), (c, d) dibit output (c — O′, d — O″).

Truth table of NOT based dibit latch

DIBIT			DIBIT		
based input I′	input I″	Digital **in**put	based output O′	output O″	Digital **o**utput
ν_1 [0]	ν_2 [1]	0	ν_2 [1]	ν_1 [0]	1
ν_2 [1]	ν_1 [0]	1	ν_1 [0]	ν_2 [1]	0

it is NOT based latch circuit. Now, if we change the input, output changes accordingly. Again, if there is no input is given at the input terminal, this simulated block holds the previous output. Now, if we apply the input in form of [ν_2][ν_2] or [1][1] (here [8][8]), which is an abnormal input combination for latch circuit, for this reason a toggle is raised shown in Fig. 5. This graphical representation of input and output are shown in the Fig. 5, which fully supports the truth table of latch circuit (Table).

4. CONCLUSIONS

As dibit representation technique is very much accurate and reliable one, it supports for reducing of bit error problem by increasing high signal to noise ratio. It can also expect high degree of parallelism. Also truth table satisfies the dibit based latch logic circuit. Therefore its performance can directly be utilized for developing and verifying the performances of different logic devices based on frequency encoding principle. Using this dibit representation one can implement for other sequential and combinational all optical operations like flip-flops, multivibrators, memories etc.

REFERENCES

1. *Pratim S.S., Satpati B., Mukhopadhyay S.* New simulative studies on performance of semiconductor optical amplifier based optical switches like frequency converter and add-drop multiplexer for optical data processors // J. Opt. 2013. V. 42. № 4. P. 360–366.
2. *Sarkar P.P., Satpati B., Mukhopadhyay S.* Analytical and simulative studies on optical NOR and controlled NOR logic gates with semiconductor optical amplifier // Optik-Intern. J. Light and Electron Optics. 2014. V. 125. № 3. P. 1333–1336.
3. *Sarkar P.P., Satpati B., Mukhopadhydy S.* Verification of all optical frequency encoded OR logic operation with its simulated result // Intern. J. Electronics & Communication Technol. 2013. V. 4. № 1. Spl. 1. P. 86–88.
4. *Dutta S., Mukhopadhyay S.* Alternating approach of implementing frequency encoded all-optical logic gates and flip-flop using semiconductor optical amplifier // Optik-Intern. J. Light and Electron Opt. 2011. V. 122. № 12. P. 1088–1094.
5. *Mukhopadhyay S.* Binary optical data subtraction by using a ternary dibit representation technique in optical arithmetic problems // Appl. Opt. 1992. V. 31. № 23. P. 4622–4623.
6. *Kim H., Kwon B., Suh M., Kang D.S., Kim Y., Jeon D.Y.* Degradation characteristics of red light-emitting $CuInS_2$/ZnS quantum dots as a wavelength converter for LEDs // Electrochem. and Solid-State Lett. 2011. V. 14. № 10. P. K55–K57.
7. *Wang K.Y., Foster A.C.* Ultralow power continuous-wave frequency conversion in hydrogenated amorphous silicon waveguides // Opt. Let. 2012. V. 37. № 8. P. 1331–1333.
8. *Ghosh B., Mukhopadhyay S.* A novel realization of all-optical dibit represented frequency encoded Boolean and quaternary inverters without switching device // Optik-Intern. J. Light and Electron Opt. 2013. V. 124. № 21. P. 4813–4815.
9. *Chandra S.K., Sarkar P.P., Biswas S., Mukhopadhyay S.* All-optical phase encoded 4-to-1 phase multiplexer using four wave mixing in semiconductor optical amplifier // Optik-Intern. J. Light and Electron Opt. 2014. V. 125. № 23 P. 6953–6957.